| Notice of Allowability | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/653,303 | KER ET AL. | |
| | Examiner | Art Unit | |
| | Thomas L Dickey | 2826 | |

***-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--***

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *AMENDMENT FILED 9/20/04*.

2. ☒ The allowed claim(s) is/are *1-5 and 7-19*.

3. ☒ The drawings filed on *02 September 2003* are accepted by the Examiner.

4. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☒ All b) ☐ Some* c) ☐ None of the:
      1. ☒ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
**THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.**

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

6. ☐ CORRECTED DRAWINGS ( as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review ( PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   **Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).**

7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

**Attachment(s)**

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

Minhloan Tran
Primary Examiner
Art Unit 2826

## REASONS FOR ALLOWANCE

1. The following is an examiner's statement of reasons for allowance:

Claims 1-5 and 7-14 are allowed over the references of record because none of these references disclosed or can be combined to yield the claimed invention such as an ESD protection circuit with high substrate-triggering efficiency comprising a multi-finger-type device having a plurality of finger gates below which parasitic BJTs are formed, a plurality of finger sources, each of which is an emitter of one of the parasitic BJTs, and at least one finger drain coupled to a pad; a plurality of voltage drop elements, each of which is coupled between one of the finger sources and a power line to detect a transient current flowing through one of the finger gates; and a plurality of feedback circuits, each of which is coupled between a base of a first parasitic BJT and an emitter of a second parasitic BJT, and activates the first BJT to bypass ESD current during an ESD event, with the further restriction that one of the finger gates is coupled to a pre-driver, as recited in claim 1, or that the voltage drop elements are inductors, as recited in claim 9, or that one of the voltage drop elements is a diode or a series of diodes, as recited in claims 10 and 11. Claims 15-19 are allowed over the references of record because none of these references disclosed or can be combined to yield the claimed invention such as an ESD protection circuit with high substrate-triggering efficiency formed on a substrate of a second conductivity comprising a guard ring of the second conductivity formed on the substrate as a contact region thereof; a plurality of fingers enclosed by the guard ring, each of which has a finger source formed by a first

doping region of a first conductivity, a finger drain formed by a second doping region of the first conductivity and coupled to a pad, a finger gate between the first and second doping region, and a substrate current input node formed by a third doping region of the second conductivity enclosed by the second doping region, wherein the first and second doping region, and the proximate substrate form a parasitic BJT; a plurality of resistors formed by wells, each of which is coupled between one of the finger sources and a power line; and internal connection circuits coupling one of the finger sources to one of the substrate current input nodes to activate a second parasitic BJT by current flowing through a first parasitic BJT and one of the resistors coupled thereto during an ESD event, as recited in claim 15.

With regard to claims 1 and 9-11 Maria Verhaege et al. 2002/0033507 discloses an ESD protection circuit with high substrate-triggering efficiency comprising a multi-finger-type device having a plurality of finger gates 906, a plurality of finger sources 904, each of which is an emitter of one of a series of parasitic BJTs formed below said finger gates 906, and at least one finger drain 902 coupled to a pad 520; a plurality of voltage drop element resistors $R_D$ formed by a well of a first conductivity in a substrate of a second conductivity, each of which is couple between one of the finger sources 904 a power line $V_{ss}$ to detect a transient current flowing through one of the finger gates 906; and a plurality of feedback circuits 908 (note figure 8D), each of which is coupled between a base of a first parasitic BJT and an emitter of a second parasitic BJT, and activates the first BJT to bypass ESD current during an ESD event. Note figures 8D, 9, 10, 17A-B,

and 19, also paragraphs 78-82 of Maria Verhaege et al. However, Maria Verhaege et al. does not disclose or suggest that one of the finger gates is coupled to a pre-driver, as recited in claim 1, or that the voltage drop elements are inductors, as recited in claim 9, or that one of the voltage drop elements is a diode or a series of diodes, as recited in claims 10 and 11.

With regard to claims 15 Maria Verhaege et al. discloses an ESD protection circuit with high substrate-triggering efficiency formed on a substrate of a second conductivity comprising a guard ring 910 of the second conductivity formed on the substrate as a contact (note the specific disclosure regarding guard ring as contact region, in paragraph 81) region thereof; a plurality of fingers enclosed by the guard ring 910, each of which has a finger source 904 formed by a first doping region 904 of a first conductivity, a finger drain formed by a second doping region 902 of the first conductivity and coupled to a pad 520, a finger gate 906 between the first 904 and second 902 doping region, and a substrate current input node formed by a third doping region of the second conductivity enclosed by the second 902 doping region, wherein the first 904 and second 902 doping region, and the proximate substrate form a parasitic BJT; a plurality of resistors $R_D$ formed by wells of the second conductivity between the first doping region and a fourth doping region coupled to a power line $V_{ss}$, each of which is coupled between one of the finger sources 904 and the power line; and internal connection circuits 908 (note figure 8D) coupling one of the finger sources 904 to one of the substrate current input nodes to activate a second parasitic BJT by current

flowing through a first parasitic BJT and one of the resistors coupled thereto during an ESD event. Note figures 8D, 9, 10, 17A-B, and 19, also paragraphs 78-82 of Maria Verhaege et al. However, as applicants point out in their paper dated 09/20/04, Maria Verhaege et al. does not disclose or suggest that the substrate current input node formed by a third doping region of the second conductivity is enclosed by the second doping (drain-forming) region, as required by claim 15, and illustrated in plan view by, for example, applicant's figures 10 and 17 (showing examples of applicants' second-doping/drain-forming region 48 enclosing applicant's substrate current input node 50).

**2.** Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

***Conclusion***

**3.** Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thomas L Dickey whose telephone number is 571-272-1913. The examiner can normally be reached on Monday-Thursday 8-6.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J Flynn can be reached on 703-308-6601. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

**TLD**
**10/2004**